SUBRANGING ANALOG-TO-DIGITAL CONVERTER WITH INTEGRATING SAMPLE-AND-HOLD

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ABSTRACT

A subranging analog-to-digital converter (ADC) includes an integrating sample-and-hold circuit. The integrating sample-and-hold circuit is configured to sample an input voltage by charging at least one capacitor by coupling a current proportional to the input voltage to the at least one capacitor. A coarsely-quantizing ADC is configured to convert the voltage on the at least one capacitor to a digitized value. A digital-to-analog converter is configured to convert the digitized value to an analog voltage. A finely-quantizing ADC is configured to convert the difference between the analog voltage and the voltage on the charged at least one capacitor in the integrating sample-and-hold circuit to another digitized value.